CLAIMS

What is claimed is:

1. A method for determining connectivity of a hierarchical circuit design, comprising steps of:

traversing hierarchical interface connections in a plurality of hierarchical blocks in at least a part of the circuit design by performing steps, for each block instance in each hierarchical block in the design, including:

for each port instance on said each block instance, wherein the port instance is not connected to a net in a parent block, generating a warning indicating the name of the port instance that is not connected; and

for each port, in each of the hierarchical blocks, that is not connected to a net within the block, generating a warning indicating the name of the port that is not connected.

2. The method of claim 1, wherein the traversing step is performed prior to an analysis of the circuit design.

3. The method of claim 1, wherein the warning comprises a message transmitted to a user terminal.

4. The method of claim 1, wherein a top hierarchical level of one of the hierarchical blocks is selected as an initial hierarchical block in the traversing step.

5. A method for determining connectivity in a plurality of hierarchical blocks of a hierarchical circuit design, comprising steps of:

traversing hierarchical interface connections of the hierarchical blocks, wherein a top hierarchical level of one of the hierarchical blocks is selected as an initial hierarchical block, by performing steps,

for each block instance in each hierarchical block in at least a part of the design, including:

for each port instance on said each block instance, wherein the port instance is not connected a net in a parent block, generating a warning indicating the name of the port instance that is not connected; and

for each port, in each of the hierarchical blocks, that is not connected to a net within the block, generating a warning indicating the name of the port that is not connected;

wherein the warning comprises a message transmitted to a user terminal.

6. The method of claim 5, wherein the traversing step is performed prior to an analysis of the circuit design.

7. A method for determining connectivity of a hierarchical circuit design, comprising steps of:

evaluating hierarchical interface connections of the design by determining, for each block instance in each of the hierarchical blocks in the design:

whether each port instance, on said each block instance, is connected a net in a parent block; and

whether each port, in each of the hierarchical blocks, is connected to a net within the block; and

generating a warning upon detection of at least one disconnected said net within the hierarchical blocks.

8. The method of claim 7, wherein the warning comprises a message transmitted to a user terminal.

9. The method of claim 7, wherein a top hierarchical level of one of the hierarchical blocks is selected as an initial hierarchical block in the evaluating step.

10. A system for determining connectivity of a hierarchical circuit design, comprising:

a processor;

a connectivity module, executable by the processor to evaluate hierarchical interface connections between hierarchical blocks in the circuit design;

a user interface module, coupled to the processor, for generating a warning upon detection of at least one disconnected net within the hierarchical blocks;

wherein the connectivity module evaluates hierarchical interface connections of the design by determining, for each block instance in each of the hierarchical blocks in the design:

whether each port instance, on said each block instance, is connected a net in a parent block, wherein a warning, indicating the name of each said port instance that is not connected, is generated by the user interface module; and

whether each port, in each of the hierarchical blocks, is connected to a net within the block, wherein a warning, indicating the name of each said port that is not connected, is generated by the user interface module.

11. The system of claim 10, further including a storage unit, accessible to the processor, in which the circuit design is stored is stored.

12. The system of claim 10, wherein a hierarchical model of the circuit design, accessible by the connectivity module via the processor, is used to indicate the hierarchical interface connections between hierarchical blocks in the circuit design.

13. A system for determining connectivity of a hierarchical circuit design, comprising:

means for evaluating hierarchical interface connections of the design by determining, for each block instance in each of the hierarchical blocks in the design:

whether each port instance, on said each block instance, is connected to a net in a parent block; and

whether each port, in each of the hierarchical blocks, is connected to a net within the block; and

means for generating a warning upon detection of at least one disconnected said net within the hierarchical blocks.

14. The system of claim 13, wherein a top hierarchical level one of the hierarchical blocks is selected as an initial hierarchical block used by said evaluating means.

15. The system of claim 13, wherein the warning comprises a message transmitted to a user terminal.

16. The system of claim 13, wherein the hierarchical interface connections are evaluated prior to an analysis of the circuit design.

17. A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for determining connectivity of a hierarchical circuit design, comprising:

evaluating hierarchical interface connections of the design by determining, for each block instance in each of the hierarchical blocks in the design:

whether each port instance, on said each block instance, is connected to a net in a parent block; and

whether each port, in each of the hierarchical blocks, is connected to a net within the block; and

generating a warning upon detection of at least one disconnected said net within the hierarchical blocks.